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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,667	05/01/2001	Subhash Gupta	54364	4777

7590 01/17/2003

The Law Offices of Calvin B. Ward  
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EXAMINER

MITCHELL, JAMES M

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 01/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/847,667	GUPTA ET AL.
	Examiner James Mitchell	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### **Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 04 September 2002 .

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) 11-16 is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-10 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)  The proposed drawing correction filed on \_\_\_\_\_ is: a)  approved b)  disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)  The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)  All b)  Some \* c)  None of:

1.  Certified copies of the priority documents have been received.
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14)  Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)  The translation of the foreign language provisional application has been received.

15)  Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)      4)  Interview Summary (PTO-413) Paper No(s). \_\_\_\_ .  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)      5)  Notice of Informal Patent Application (PTO-152)  
3)  Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_ .      6)  Other: \_\_\_\_ .

## DETAILED ACTION

### ***Election/Restrictions***

The restriction requirement was set out in the office action filed March 13, 2002. During a telephone conversation with Calvin Ward on February 25, 2002 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-10. Affirmation of this election was required to be made in applicant's response filed September 4, 2002. Applicant must make affirmation in next reply to this Office action or the reply will be found non-responsive. Claims 11-16 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5 and 7 are rejected under 35 U.S.C. 102(B) as being anticipated by Cambou et al. (US 5,091,330).

Cambou (Fig 1-5) discloses a substrate (12,10) comprising a wafer material (12) said substrate having a first (top) and second (bottom) surfaces, said first surfaces having a circuit layer (Col. 3, Lines 62-67) constructed thereon, a plurality of vias (trench defined by section between 13 & 14) extending a first distance from said first surface of said substrate into said substrate, said first distance being less than the distance

between said first and second surfaces of said substrate, said vias having a bottom surface comprising an insulating stop layer (15) that is more resistant to CMP than said wafer material ( Col. 3, Lines 41-45); with an electrically insulating silicon dioxide layer (16; Col.2, Line 56) having a top and bottom surfaces, said dielectric covering said circuit layer such that a bottom surface is contact with said integrated; with said vias filled with an electrically conducting material (31).

(e) the invention was described in-  
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or  
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-2 and 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakano et al. (US 2001/0030366).

Nakano et al. (Fig 10a-10h) discloses a substrate comprising a wafer material (10a; Par. 0133) said substrate having a first (top) and second (bottom) surfaces, said first surfaces having a circuit layer (Par 0004) constructed thereon, a plurality of vias (not labeled) extending a first distance from said first surface of said substrate into said substrate, said first distance being less than the distance between said first and second surfaces of said substrate, said vias having a bottom surface comprising a tungsten etch stop layer(3; Par 0007) comprising a stop material that is inherently more resistant to CMP than said wafer material; with an electrically insulating silicon dioxide layer (4 Par 0037) having a top and bottom surfaces, said dielectric covering said circuit layer such that a bottom surface is contact with said integrated, and a plurality of inherent

electrical conductors (6) buried in said dielectric layer and making electrical connections to said integrated circuit elements; wherein at least one vias (10) extends through said dielectric layer and whereon one of said vias is filled with an electrically conducting material with said via terminating in an inherent electrically conducting pad on said top surface of the dielectric layer (shown in Fig 10g; via top portion of conductor, 6), said pad extends above said top surface (via top portion above hole,10) of said dielectric layer and the electrical connector is connected electrically to said one of said vias.

Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 6,461,937).

Kim (Fig 17) discloses a substrate comprising a wafer material (200) said substrate having a first (top) and second (bottom) surfaces, said first surfaces having a circuit layer (Col. 1, Lines 19-21) constructed thereon, a plurality of vias (not labeled; Col. 3, Line 21) extending a first distance from said first surface of said substrate into said substrate, said first distance being less than the distance between said first and second surfaces of said substrate, said vias having a bottom surface comprising a stop layer (212) comprising a stop material that is more resistant to CMP than said wafer material; with an electrically insulating silicon dioxide layer (210; Col. 8, Line 7) having a top and bottom surfaces, said dielectric (202, 210) covering said circuit layer such that a bottom surface is contact with said integrated .

Claims 1, 3, 5 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lopatin et al. (US 6,433,379).

Lopatin (Fig 1-3) discloses a substrate (20) comprising a wafer material (20b) said substrate having a first (top) and second (bottom) surfaces, said first surfaces having a circuit layer (Col. 1, Line 1) constructed thereon, a plurality of vias (30) extending a first distance from said first surface of said substrate into said substrate, said first distance being less than the distance between said first and second surfaces of said substrate, said vias having a bottom surface comprising a tantalum stop layer (40) that is more resistant to CMP than said wafer material; with an electrically insulating silicon dioxide layer (20a) having a top and bottom surfaces, said dielectric covering said circuit layer such that a bottom surface is contact with said integrated; with said vias lined with a layer of insulating material(42) filled with a copper electrically conducting material (38).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

  
jmm  
January 13, 2003



DAVID E. GRAYBILL  
PRIMARY EXAMINER